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SIMULATION OF ENHANCED PULSE TRIGGERED FLIP FLOP WITH HIGH PERFORMANCE APPLICATIONS

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ABSTRACT

Flip-flops are the major storage elements in all system on chip (SOC) of digital design and one of the most power consumption components. It is important to reduce power dissipation in clock distribution networks and flip-flops. The power delay is mainly due to clock delays. The delay of flip-flops should be minimized for efficient implementation. This paper designed Enhanced Pulse Triggered Flip Flop (D-FF) based different applications (4 bit PIPO, 4bit SISO and 3 bit Asynchronous ripple counter). The design significantly reduces the power dissipation. Performances of all the circuits are investigated power consumption using TSMC 180nm technology.

KEYWORDS: Delay, full adder, Power Delay, XOR Gate.

INTRODUCTION

The most important prime mover of low power research and design is our convergence to a mobile society. We are moving from desktops to laptops to handhelds and smaller computing systems. With this profound trend continuing, and without a matching trend in battery life expectancy, the more low power issues will have to be addressed. This entails that low power tools and methodologies have to be developed and adhered to. The current trends will eventually mandate low power design automation on a very large scale to match the trends of power consumption of today's integrated chips.

Since the flip-flops are the essential elements for designing the [3] semiconductor devices, they have a crucial influence on determining the parameters like speed, power consumption, clock skew tolerance and layout area. Timing elements i.e. latches and flip-flops are critical for the performance [4] of the digital systems because of the tight time constraints and requirements of low power. In many digital VLSI designs, the clock system consists of clock distribution network and flip-flops. By its action as timing signal the system controls the working rhythm of the chip. The digital system basically consists of set of flip-flops and interconnected combinational logic, the synchronous clock signal controls all flip-flops for sampling and storing their data synchronously.

Outline this paper

The rest of the paper is organized as follows: In section II, we describe Enhanced pulse Triggered Flip flop. In section III, some standard implementations of the full adder cell is discussed as previous work. In section IV, the proposed full adder cell is described. In section V, simulation results for proposed and existing designs are given and comparisons are carried out.

PULSE TRIGGERED FLIP FLOPS

For higher performance, the pulse triggered flip flops are the fastest alternatives among all the flip flop types [2]. A P-FF consists of a pulse generator for generating strobe signals and latch for data storage. Since triggering pulses generated on the transition edge of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF.

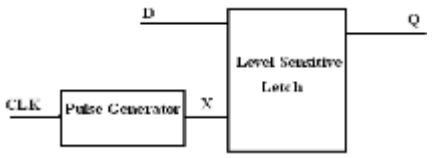

Fig 1: Block diagram of Pulse triggered flip flop

The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master-slave configuration, is needed. Depending on the method of pulse generation, P-FF design can be classified as implicit or explicit. in an implicit type P-FF ,the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In an explicit type P-FF, the design of pulse generator and

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latch are separate [1]. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. Implicit type designs, however, face a lengthened discharging path in latch design, which leads to inferior timing characteristics. Explicit type P-FF designs face a similar pulse width control issue, but the problem is further complicated in the presence of a large capacitive load, e.g., when one pulse generator is shared among several latches. Pulse triggered flip flops reduce the two stages into one stage and are characterized by the soft edge property. Due to these timing issues, P-FFs provide higher performance than their master slave counterparts, and since we are concerned about performance, MS FFs will not be discussed any further in this paper. P-FFs outperform hard-edged FFs, as they provide a soft edge, negative setup time, and small to delays, which help not only in reducing the delay penalty this flip flops incur on cycle time but also help in absorbing the clock skew.

ENHANCED PULSE TRIGGERED LOW-POWER FLIP FLOP (EPTL -FF) [5]

Figure.2 shows our design Enhanced Pulse Triggered Flip Flop (EPTFF), for high speed operation of data storage and a popular alternative to Master slave flip-flop. The enhanced pulse triggered low-power flip flop (EPTLFF) with pulse control scheme consists of pulse generator for generating Strobe signals and a latch for data storage. It reduces the number of transistors stacked in the discharging path and also reduces the overall switching delay.

The upper part latch design and lower part enhanced pulse generation. This particular clock pulse is used to input pass transistor logic, N2 input pass transistor logic to control the discharge of transistor N1. The output node Z is kept at zero most of the time. At the rising edges of the clock, transistors N2 is turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1.The switching power at node Z can be reduced due to a diminished voltage swing. Where the discharge control signal is driven by a single transistor, conduction of one NMOS transistors (N2) speeds up the operations of pulse generation. In this design reduced the discharging path X, avoids unnecessary internal node transitions to reduce power consumption and power delay product.

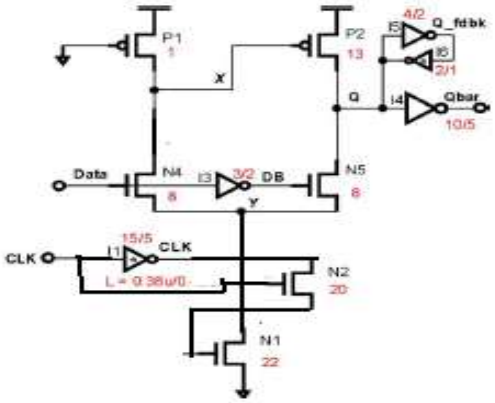

Fig. 2 Enhanced Pulse Triggered Flip Flop [5]

SHIFT REGISTER

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states. The storage capacity of a register is the total number of bits (1 or 0) of digital data it can retain. Each stage (flip flop) in a shift register represents one bit of storage capacity

Parallel in Parallel out

For parallel in parallel out shift registers, all data bits appear

On the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit parallel in parallel out shift register constructed by d flip-flops and shown in fig. 5.

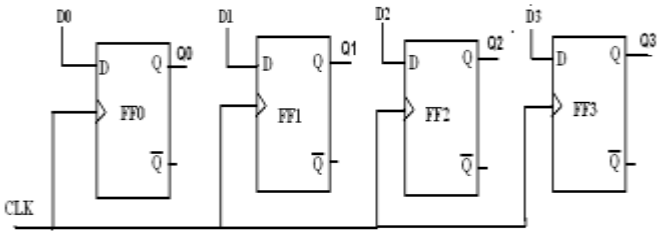

Figure.4. 4 Bit Parallel-in Parallel-out (PIPO)

Serial in Serial out

For Serial in Serial out shift registers, all data bits appear

on the Serial outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit Serial in Serial out shift register constructed by d flip-flops and shown in fig. 5

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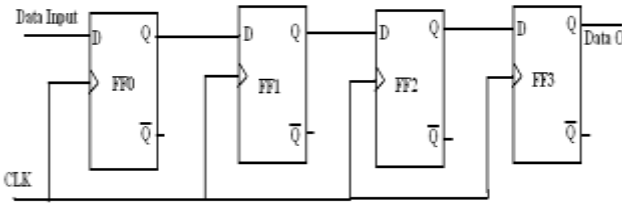

Figure.5. 4 Bit Serial-in Serial-out (SISO)

3bit asynchronous counter

Flip-flops can be connected in series, as shown in Figure 5. The resulting outputs are given in Figure 9. Hence, this is a 3-bit counter, with maximum count 23-1 = 7. It is clearly possible to expand such a counter to an indefinite number of bits. While asynchronous counters are easy to assemble, they have serious drawbacks for some applications. In particular, the input must propagate through the entire chain of flip-flops before the correct result is achieved. Eventually, at high input rate, the two ends of the chain, representing the LSB and MSB, can be processing different input pulses entirely.

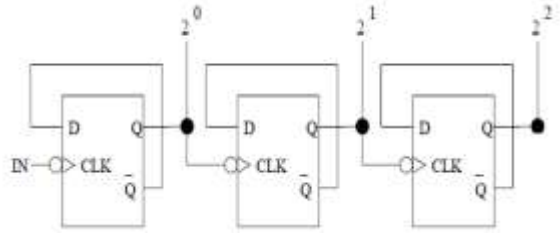

Figure 6: bit Asynchronous (\ripple") counter made from cascaded D-type

SIMULATION RESULTS

The power consumption results are summarized in Table I.

Due to a shorter discharging path and the employment of a

conditional pulse enhancement scheme, the power consumption of the proposed design is the lowest in all tests

patterns.

Table: 1 Comparisons table

Circuit	Power consumption (pW
EPTL	.17
4 BIT PIPO	6.2
4 BIT SISO	.14
3 BIT Ripple Asyn. Counter	5.2

To evaluate the performance, shift registers discussed in this paper are designed using 180-nm CMOS technology. All simulations are carried out using Tanner Tools simulation at nominal conditions with 1GHz frequency range. Flip-flop based PIPO, SISO Shift Register and 3 bit Asynchronous ripple counter are shown in figure. 7. 8 & 9.

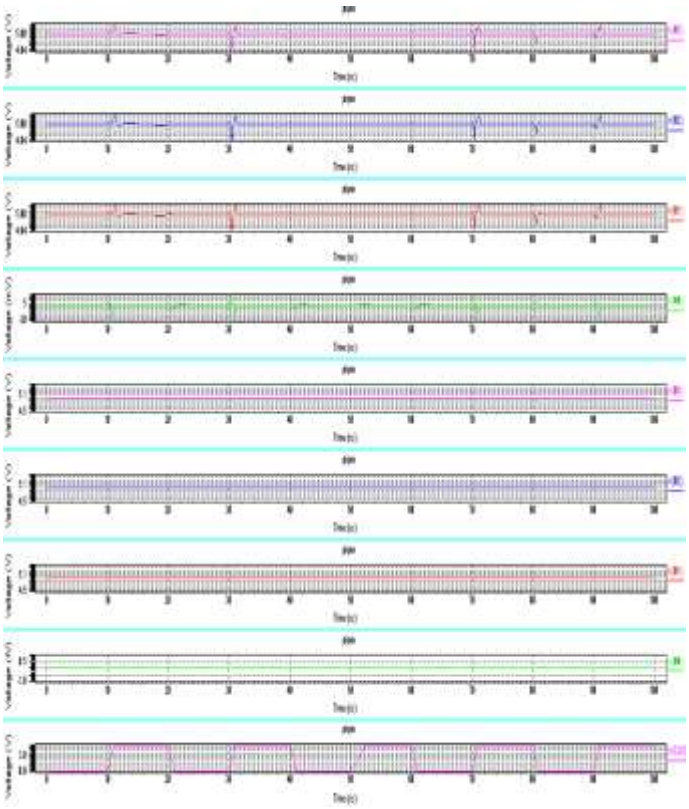

Figure.7. Output Waveform of PIPO

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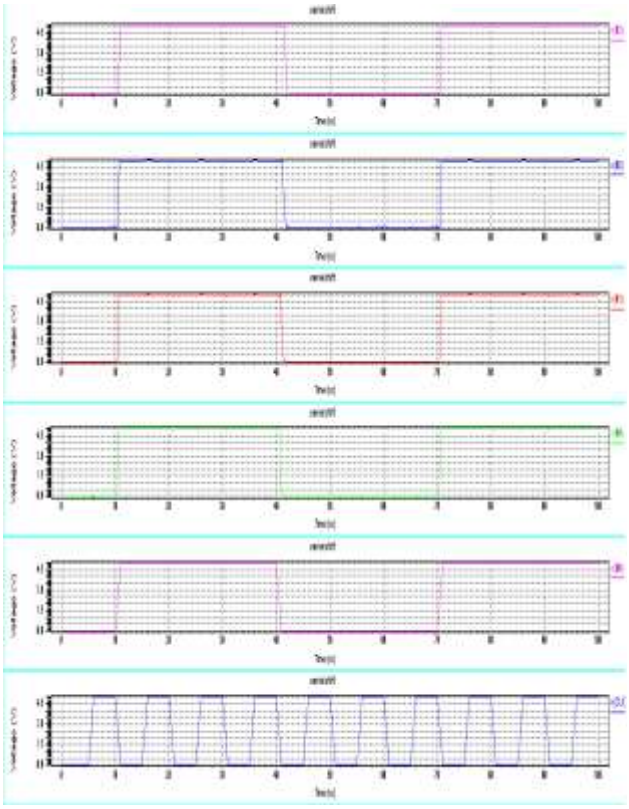

Figure8. Output Waveform of Serial Input Serial output

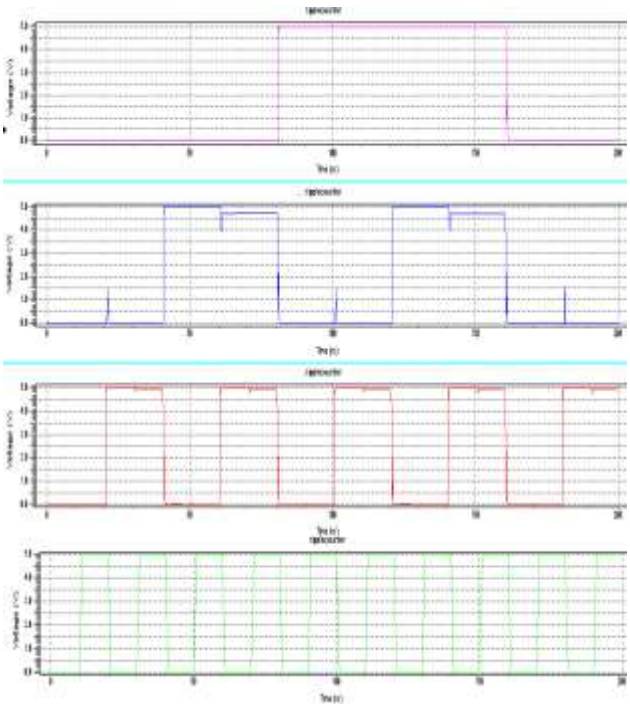

Figure .9.Wave form 3bit Asynchronous Counter made from cascaded D-type

CONCLUSION

This paper concludes that EPTL Flip-Flop designed with 16 transistors is having less power consumption. The Flip-Flops are simulated for 180nm technology using the Tanner Tool. The comparisons of 4bit Parallel in Parallel out, 4 bit serial in serial out Shift Register and 3 bit asynchronous counter are shown in Table 1 to verify the designed methods using TSMC 180-nm technology. In such circuits where the performance and power are high volatile constraints the devices with better the performance with low power are much essential and this paper achieves the simple P-FF design with reduction in power consumption that of EPTL based application.

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